Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VIN-**
2. **VIN+**
3. **N/C**
4. **VOUT**
5. **–VS**
6. **+VS**
7. **N/C**

**.039”**

**1 7**

**6**

**5**

**4**

**2 3**

**.034”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: -VS**

**APPROVED BY: DK DIE SIZE .034” X .039” DATE: 4/19/21**

**MFG: TEXAS / BURR THICKNESS .015” P/N: OPA656**

**DG 10.1.2**

#### Rev B, 7/1